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EXAMINER	
PHILPOTT, JUSTIN M	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 03/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/553,966	WARD, KENNETH A.	
	Examiner	Art Unit	
	Justin M Philpott	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed January 9, 2004 have been fully considered but they are not persuasive.

2. Regarding claim 1, first, applicant argues (pages 15-16) that Christensen does not teach the lowest level of the hierarchical channel map comprises one bit for each communication channel supported by the host adapter wherein each bit indicates whether the communication channel to which it is mapped has a pending communication request as recited in claim 1. However, as discussed in the previous action, and repeated herein, Christensen teaches a first memory (e.g., channel interrupt queues Q0-Q7 within main storage 23) configured to store a lowest level of a hierarchical channel map, wherein the lowest level comprises one bit for each communication channel supported by the host adapter (e.g., each entry in a queue corresponds to a channel interrupt), wherein each bit of the lowest level is set to indicate that the communication channel to which it is mapped has a pending communication request and is cleared if the communication channel to which it is mapped does not have a pending communication request (e.g., see col. 6, lines 3-17). Applicant further argues that, in Christensen, "once an interrupt request has been remove[d] from a queue, the same I/O channel may or may not have another interrupt request pending in a different queue entry or even a different queue", and that "once an interrupt request has been remove[d] from a queue, the same queue entry can be used to store an interrupt request from a completely different I/O channel." Applicant appears to be arguing that each queue entry (or vacancy) in Christensen is not dedicated to only one specific channel as in

applicant's invention. However, such a feature is not evident in applicant's claim 1. While applicant may choose to amend claim 1 to include such a feature, e.g., by reciting, "wherein said lowest level comprises, for each communication channel supported by said host adapter, one bit dedicated only for the corresponding communication channel to which it is mapped", Christensen anticipates claim 1 as presently written. That is, Christensen anticipates the lowest level comprises one bit for each communication channel supported by the host adapter (e.g., each entry in a queue corresponds to a channel interrupt). Thus, applicant's argument is not persuasive.

Second, applicant argues (page 16, first paragraph – page 17, first paragraph) that Christensen does not teach a host adapter configured to determine a next channel to be serviced by examining the hierarchical channel map as recited in claim 1. However, as discussed in the previous action, and repeated herein, Christensen teaches the host adapter (e.g., channel controller 24) is configured to determine a next channel to be serviced by examining the hierarchical channel map (e.g., channel controller 24 generates SIGI command which identifies the queue on which an entry will be posted for a received interrupt, wherein entries are serviced according to the order in which they are placed on the queue, see col. 5, line 65 – col. 6, line 17). That is, Christensen teaches the host adapter (e.g., channel controller 24) examines the hierarchical channel map (e.g., comprising Q0-Q7 within MS 23) by identifying a queue (e.g., one of Q0-Q7) to which an entry is to be placed (e.g., see col. 6, lines 3-11) and thus determines a next channel to be serviced by such queue entry. Additionally, applicant argues that Christensen teaches a PND register 46 in combination with a central processor and system controller 22 select a queue. However, the action performed by the channel controller 24 is

necessary for the determining of a next channel to be serviced (e.g., via generating SIGI command for identifying the queue on which an entry is posted as a pending interrupt which will next be serviced, see col. 5, line 65 – col. 6, line 39). Further, the functioning of PND register 46 asserted by applicant requires the SIGI command generated by the channel controller 24 (e.g., see col. 6, lines 35-39). Thus, applicant's argument is not persuasive.

3. Regarding claim 12, first applicant argues (page 17, second paragraph continued to page 18) that Christensen does not teach selecting a set bit in the top level of the hierarchical channel map, wherein the bit indicates a group of bits in a next level of the map to examine as recited in claim 12. However, as discussed in the previous action, and repeated herein, comparable to claim 1, Christensen teaches selecting a bit in a top level of a hierarchical channel map which indicates a group of bits in a next level of the hierarchical channel map to examine. That is, Christensen teaches a second memory (e.g., pending register 46) configured to store a top level of the hierarchical channel map, wherein each bit of the top level (e.g., bits PND(0) – PND (7)) maps to a section of the lowest level (e.g., each PND bit maps to a particular one of queues Q0-Q7), wherein each bit of the top level is set if at least one bit in the section of the lowest level to which it is mapped is set and is cleared if none of the bits in the section of the lowest level to which it is mapped are set (e.g., see col. 6, lines 24-50).

Second, applicant argues (page 18, first paragraph) that Christensen does not teach examining in each intermediate level only a group of bits indicated by the set bit selected in the previous level as recited in amended claim 12. Applicant's argument with respect to amended claim 12 has been considered but is moot in view of the new ground(s) of rejection.

Third, applicant argues (page 18, second paragraph) that Christensen does not teach examining in the lowest level as recited in claim 12. However, as discussed above, Christensen teaches the host adapter (e.g., channel controller 24) examines the hierarchical channel map (e.g., comprising Q0-Q7 within MS 23) by identifying a queue (e.g., one of Q0-Q7) to which an entry is to be placed (e.g., see col. 6, lines 3-11) and thus determines a next channel to be serviced by such queue entry.

4. Regarding claim 29, first, applicant argues (page 18, third paragraph continued to page 19) that Christensen does not teach a computer readable medium as recited in claim 29. However, in response to applicant's arguments, the recitation of a computer readable medium has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). Thus, applicant's argument is moot.

Second, applicant argues (page 19, first paragraph) that Christensen does not teach top, second and bottom level service masks as recited in claim 29. Applicant's argument with respect to claim 29 has been considered but is moot in view of the new ground(s) of rejection.

5. Regarding claim 30, applicant argues (page 19, second paragraph continued to page 20) that Christensen does not teach examining a portion of intermediate levels as recited in claim 30. Applicant's argument with respect to claim 30 has been considered but is moot in view of the new ground(s) of rejection.

6. Regarding claim 31, first, applicant argues (page 20, first paragraph) that Christensen does not teach organization into channel section as recited in claim 31. Applicant's argument with respect to claim 31 has been considered but is moot in view of the new ground(s) of rejection.

Second, applicant argues (page 20, second paragraph) that Christensen does not teach examining no more of the lowest level than a portion as recited in claim 31. However, as discussed above, Christensen teaches the host adapter (e.g., channel controller 24) examines the hierarchical channel map (e.g., comprising Q0-Q7 within MS 23) by identifying a queue (e.g., one of Q0-Q7) to which an entry is to be placed (e.g., see col. 6, lines 3-11) and thus determines a next channel to be serviced by such queue entry.

Allowable Subject Matter

7. The indicated allowability of claims 2-6 is withdrawn for reasons discussed in the following action.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1, 9-11, 18-23 and 25-28 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,271,468 to Christensen et al.

Regarding claims 1 and 18, Christensen teaches a system for servicing a plurality of communication channels, comprising: a host adapter (e.g., channel controller 24 in FIG. 1) configured to service communication requests (e.g., I/O interrupt requests) from communication requestors (e.g., I/O devices via control units 26, 27) to communication targets (e.g., central processors 20, 21), wherein the host adapter (e.g., channel controller 24) provides for up to a maximum number of communication channels to service the communication requests; a communication fabric (e.g., system controller 22) configured to provide a limited bandwidth to the host adapter to service the communication requests, wherein the communication fabric (e.g., 22) couples the communication targets (e.g., 20, 21) to the host adapter (e.g., 24); a first memory (e.g., channel interrupt queues Q0-Q7 within main storage 23) configured to store a lowest level of a hierarchical channel map, wherein the lowest level comprises one bit for each communication channel supported by the host adapter (e.g., each entry in a queue corresponds to a channel interrupt), wherein each bit of the lowest level is set to indicate that the communication channel to which it is mapped has a pending communication request and is cleared if the communication channel to which it is mapped does not have a pending communication request (e.g., see col. 6, lines 3-17); a second memory (e.g., pending register 46) configured to store a top level of the hierarchical channel map, wherein each bit of the top level (e.g., bits PND(0) – PND (7)) maps to a section of the lowest level (e.g., each PND bit maps to a particular one of queues Q0-Q7), wherein each bit of the top level is set if at least one bit in the section of the lowest level to which it is mapped is set and is cleared if none of the bits in the section of the lowest level to which it is mapped are set (e.g., see col. 6, lines 24-50); wherein the host adapter is configured to determine a next channel to be serviced by examining the hierarchical channel

map (e.g., channel controller 24 generates SIGI command which identifies the queue on which an entry will be posted for a received interrupt, wherein entries are serviced according to the order in which they are placed on the queue, see col. 5, line 65 – col. 6, line 17).

Regarding claims 9 and 25, Christensen teaches the system as discussed above regarding claims 1, 12-14, 18 and 31-36 and further teaches a plurality of service class masks (e.g., I/O mask 51 comprising mask bits, see col. 6, lines 56-67), wherein each service class mask is configured to map a number of the communication channels to one of a plurality of service classes (e.g., mask bits configure communication channels to one of a plurality of queues wherein each queue has a designated priority, see col. 6, lines 51-59), wherein each service class (e.g., designated priority of the queue) is allocated a portion of the limited bandwidth on the communication fabric.

Regarding claims 10 and 26, Christensen further teaches a service array (e.g., QID register 82) comprising a plurality of entries, wherein each entry indicates one of the service classes to be serviced during a current service unit (e.g., see col. 17, lines 22-30), wherein the service classes are selected in a repeating order according to the entries in the service array, and wherein the next channel to be serviced is selected from the current service class (e.g., see col. 9, line 24 – col. 10, line 31).

Regarding claims 11 and 27, Christensen further teaches for each service class a service mask for each level of the hierarchical channel map (e.g., via I/O mask 51 comprising mask bits, see col. 6, lines 56-67), wherein when its corresponding service class is being serviced each service mask indicates the next bit position to be examined within a selected group of bits to determine a selected group of bits to be examined at the next level (e.g., within the designated

queue having the highest non-empty priority), except wherein the service mask for the lowest level indicates the next bit position to be examined within a selected group to determine the next channel with a pending request to be services (e.g., mask bits indicating the next enabled PND bit to be examined).

Regarding claim 19, Christensen further teaches the host adapter (e.g., CC 24) is configured to service for one service unit a channel request (e.g., I/O interrupt request) from a channel mapped to a set bit at the lowest level (e.g., an entry among one of the groups of Q0-Q7) of the hierarchical channel map, wherein the set bit is selected by examining a current group of bits at the lowest level of the hierarchical channel map to select a next set bit in that group indicating a channel with a pending request (e.g., a next entry within the designated queue among Q0-Q7), and if no more bits are set in the current group (e.g., the designated queue is empty), examining a current group at the next higher level (e.g., examine next bit of the PND register 46) to select a next set bit (e.g., next bit among PND(0)-PND(7)) and then examining the next lower level group (e.g., next queue among Q0-Q7 corresponding to the selected PND bit) indicated by the selected higher level set bit.

Regarding claim 20, as discussed above regarding claims 11, 15, 17 and 27, Christensen teaches a service mask for each level of the hierarchical channel map (e.g., via I/O mask 51 comprising mask bits, see col. 6, lines 56-67), wherein each service mask is configured to indicate the next bit position in the current group to be examined for a set bit (e.g., within the designated queue having the highest non-empty priority).

Regarding claim 21, Christensen further teaches each service mask (e.g., via I/O mask 51) is configured to indicate the bit position within the group for the corresponding level of the

last selected set bit in that group (e.g., mask 51 indicates the bit position of PND, see col. 6, lines 51-68), wherein the host adapter (e.g., CC 24) is configured to examine each group for the next set bit after the bit position indicated by the corresponding service mask (e.g., see col. 6, lines 24-50).

Regarding claim 22, Christensen further teaches each group of bits at one level of the hierarchical channel map has the same number of bits (e.g., each entry in top level, PND register 46, comprises one bit).

Regarding claim 23, Christensen further teaches each group of bits at the lowest level (e.g., groups Q0-Q7) is accessible by a single memory access (e.g., see col. 9, line 24 – col. 10, line 21).

Regarding claim 28, Christensen teaches a service unit is a quantum smaller than a maximum message size for the channel requests (e.g., I/O interrupt request) (e.g., see col. 5, line 63 – col. 6, line 50, wherein a message size of the interrupt request, SIGI, exceeds the size of a interrupt request entry in the queues Q0-Q7).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 2-8, 12-17, 24 and 29-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Christensen.

Regarding claims 2, 12-14 and 29, Christensen teaches a system as described above regarding claim 1, however, may not specifically disclose one or more intermediate stages between the highest level and lowest level stages. However, it is generally considered to be within the ordinary skill in the art to duplicate parts for a multiplied effect. St. Regis Paper Co. v. Bemis Co., Inc., 193 USPQ 8, 11 (7th Cir. 1977). The stages of Christensen provide for an organized system, and accordingly, at the time of the invention it would have been obvious to one of ordinary skill in the art to include additional organizational stages within the hierarchy of Christensen in order to provide additional organization for a multiplied effect. That is, at the time of the invention it would have been obvious to one of ordinary skill in the art to include one or more intermediate stages in the hierarchical channel map of Christensen since it is generally considered to be within the ordinary skill in the art to duplicate parts for a multiplied effect.

Further, regarding claim 29, Christensen teaches the system as discussed above regarding claims 1, 12-14, 18 and 31-36 and further teaches a plurality of service class masks (e.g., I/O mask 51 comprising mask bits, see col. 6, lines 56-67), wherein each service class mask is configured to map a number of the communication channels to one of a plurality of service classes (e.g., mask bits configure communication channels to one of a plurality of queues wherein each queue has a designated priority, see col. 6, lines 51-59), wherein each service class (e.g., designated priority of the queue) is allocated a portion of the limited bandwidth on the communication fabric.

Regarding claim 3, Christensen teaches the host adapter (e.g., CC 24) is configured to service for one service unit a channel request (e.g., I/O interrupt request) from a channel mapped to a set bit at the lowest level (e.g., an entry among one of the groups of Q0-Q7) of the

hierarchical channel map, wherein the set bit is selected by examining a current group of bits at the lowest level of the hierarchical channel map to select a next set bit in that group indicating a channel with a pending request (e.g., a next entry within the designated queue among Q0-Q7), and if no more bits are set in the current group (e.g., the designated queue is empty), examining a current group at the next higher level (e.g., examine next bit of the PND register 46) to select a next set bit (e.g., next bit among PND(0)-PND(7)) and then examining the next lower level group (e.g., next queue among Q0-Q7 corresponding to the selected PND bit) indicated by the selected higher level set bit.

Regarding claims 4, 5 and 15, Christensen teaches a plurality of service class masks (e.g., I/O mask 51 comprising mask bits, see col. 6, lines 56-67), wherein each service class mask is configured to map a number of the communication channels to one of a plurality of service classes for determining next servicing (e.g., mask bits configure communication channels to one of a plurality of queues wherein each queue has a designated priority, see col. 6, lines 51-59). Further, Christensen teaches a service mask for each level of the hierarchical channel map (e.g., via I/O mask 51 comprising mask bits, see col. 6, lines 56-67), wherein each service mask is configured to indicate the next bit position in the current group to be examined for a set bit (e.g., within the designated queue having the highest non-empty priority).

Regarding claim 6, Christensen teaches a service unit is a quantum smaller than a maximum message size for the channel requests (e.g., I/O interrupt request) (e.g., see col. 5, line 63 – col. 6, line 50, wherein a message size of the interrupt request, SIGI, exceeds the size of a interrupt request entry in the queues Q0-Q7).

Regarding claims 7 and 37, Christensen teaches the system of claim 1 as discussed above and, further, teaches the first memory (e.g., Q0-Q7) and the second memory (e.g., PND(0)-PND(7)) are accessible by the host adapter (e.g., CC 24 accesses memory comprised within SC 22 and MS 23). While Christensen may not specifically require both first and second memory to be located on a same memory block, it is generally considered to be within the ordinary skill in the art to shift the location of parts absent a showing of unexpected results. Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to shift the location of the second memory (e.g., PND) from its current memory position to a memory block comprising the first memory (e.g., Q) since it is generally considered to be within the ordinary skill in the art to shift the location of parts absent a showing of unexpected results. The contention of obvious choice in design can be overcome if Applicant establishes unexpected results. In re Japikse, 86 USPQ 70 (CCPA 1950).

Regarding claims 8, 24 and 38, Christensen teaches the system of claims 1, 18 and 31-36 as discussed above and, further, teaches the second memory (e.g., PND register 46) is a register comprised within an integrated circuit (e.g., within 22). While Christensen may not specifically require that the integrated circuit comprising the second memory is specifically located within the host adapter (e.g., 24), it is generally considered to be within the ordinary skill in the art to shift the location of parts absent a showing of unexpected results. Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to shift the location of an integrated circuit comprising the second memory from its current position to a position within the host adapter (e.g., 24), since it is generally considered to be within the ordinary skill in the art to shift the location of parts absent a showing of unexpected results. The contention of obvious

choice in design can be overcome if Applicant establishes unexpected results. In re Japikse, 86 USPQ 70 (CCPA 1950).

Regarding claim 16, Christensen teaches the system as discussed above regarding claims 1, 12-14, 18 and 31-36 and further teaches a plurality of service class masks (e.g., I/O mask 51 comprising mask bits, see col. 6, lines 56-67), wherein each service class mask is configured to map a number of the communication channels to one of a plurality of service classes (e.g., mask bits configure communication channels to one of a plurality of queues wherein each queue has a designated priority, see col. 6, lines 51-59), wherein each service class (e.g., designated priority of the queue) is allocated a portion of the limited bandwidth on the communication fabric. Christensen further teaches a service array (e.g., QID register 82) comprising a plurality of entries, wherein each entry indicates one of the service classes to be serviced during a current service unit (e.g., see col. 17, lines 22-30), wherein the service classes are selected in a repeating order according to the entries in the service array, and wherein the next channel to be serviced is selected from the current service class (e.g., see col. 9, line 24 – col. 10, line 31).

Regarding claim 17, Christensen teaches for each service class a service mask for each level of the hierarchical channel map (e.g., via I/O mask 51 comprising mask bits, see col. 6, lines 56-67), wherein when its corresponding service class is being serviced each service mask indicates the next bit position to be examined within a selected group of bits to determine a selected group of bits to be examined at the next level (e.g., within the designated queue having the highest non-empty priority), except wherein the service mask for the lowest level indicates the next bit position to be examined within a selected group to determine the next channel with a

pending request to be services (e.g., mask bits indicating the next enabled PND bit to be examined).

Regarding claims 30-36, Christensen teaches a system as discussed above regarding claim 1, however, may not specifically disclose channels are further organized into channel sections or one or more intermediate stages are placed between the highest level and lowest level stages. However, it is generally considered to be within the ordinary skill in the art to duplicate parts for a multiplied effect. St. Regis Paper Co. v. Bemis Co., Inc., 193 USPQ 8, 11 (7th Cir. 1977). The stages of Christensen provide for an organized system, and accordingly, at the time of the invention it would have been obvious to one of ordinary skill in the art to include additional organizational stages, e.g., organized channels into sections or one or more intermediate stages, within the hierarchy of Christensen in order to provide additional organization for a multiplied effect. That is, at the time of the invention it would have been obvious to one of ordinary skill in the art to include an additional organizational layer in the form of channel sections in the hierarchical channel map of Christensen since it is generally considered to be within the ordinary skill in the art to duplicate parts for a multiplied effect.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin M Philpott whose telephone number is 703.305.7357. The examiner can normally be reached on M-F, 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy D Vu can be reached on 703.308.6602. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Justin M Philpott

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